FIG. 1A

1

L0	INNER	SPARE	USER DATA	SPARE	OUTER
	AREA 0	AREA 1	AREA 1	AREA 2	AREA 0

FIG. 1B

	DATA AREA 1						
L0	INNER	SPARE	USER DATA	SPARE	OUTER		
	AREA 0	AREA 1	AREA 1	AREA 2	AREA 0		
L1	INNER	Spare	USER DATA	SPARE	OUTER		
	AREA 1	AREA 4	AREA 2	AREA 3	AREA 1		

FIG. 2

	•••	
·	DMA 2	
INNER AREA	RECORDING CONDITION TEST AREA	
0	TDMA 1	
	DMA 1	
	•••	
	SPARE AREA 1	
DATA AREA	USER DATA AREA 1	
0	SUB SPARE AREA 2	SPARE AREA2
	TDMA 2	SPARE AREAZ
	•••	
OUTED ADEA	DMA 3	
OUTER AREA	•••	
	DMA 4	
	•••	

FIG. 3A

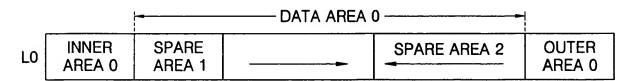


FIG. 3B

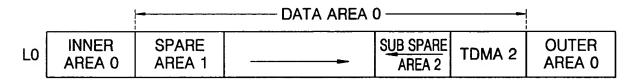


FIG. 4A

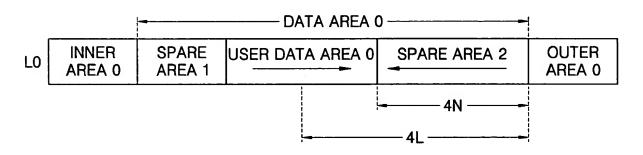


FIG. 4B

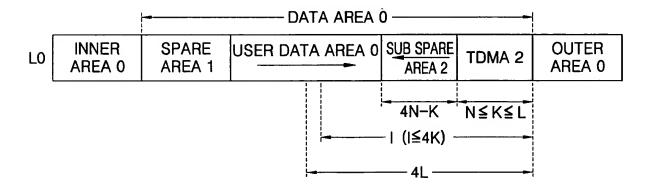


FIG. 5A

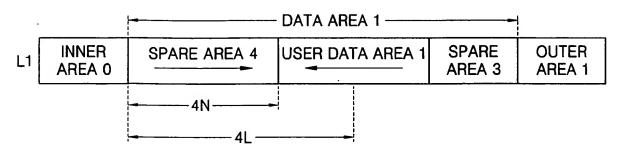


FIG. 5B

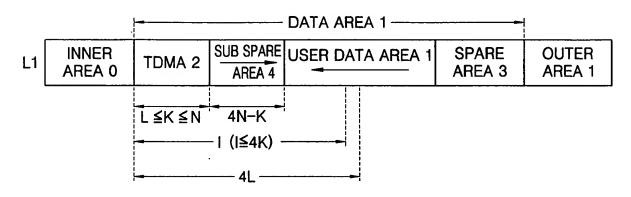


FIG. 6

